REMARKS

This Amendment and Response to Final Office Action is being submitted in response to the final Office Action mailed September 10, 2008. Claims 1-22 are pending in the Application. Claims 1, 5, and 9 are the independent claims.

Claim 5 is objected to because of informalities.

Claims 1-22 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Claims 1-2, 12-14, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Juniper ("Juniper Networks M40 Internet Backbone Router Inter-Operating With the CIENA MultiWave Sentry DWDM System") in view of the admitted prior art, Waschka, Jr. (U.S. Patent No. 4,449,247), Bach *et al.* (U.S. Patent No. 6,606,354), Bergano *et al.* ("Margin measurements in optical amplifier systems") and Hoogerbrugge ("Optimizing test strategies for SONET/SDH/ATM network element manufacturing").

Claims 3-11, 15-19, and 21-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Juniper in view of the admitted prior art, Waschka, Jr., Bach, Bergano *et al.*, and Hoogerbrugge as applied to Claim 1, and in further view of Bullock *et al.* (U.S. Patent No. 5,764,651).

In response to these rejections, Claims 1, 5, 9, 17, 19, and 22 have been amended herein to further clarify the subject matter which Applicants regard as their invention, without prejudice or disclaimer to continued examination on the merits. These amendments are fully supported in the Specification, Drawings, and Claims of the Application and no new matter has been added. Based upon the amendments, reconsideration of the Application is respectfully requested, without further search, in view of the following remarks.

Claim 5 – Objection

Claim 5 is objected to because of informalities. Accordingly, Applicants have amended Claim 5 as recited under §1 in the final Office Action and Applicants respectfully request withdrawal of this objection.

Claims 1-22 - §112, first paragraph, Rejections

Claims 1-22 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Based on Examiner's suggestions in §4 and §5 of the Non-Final Office Action, Applicants have amended Claims 1, 5, and 9, and Applicants respectfully request withdrawal of these rejections.

Claims 1-2, 12-14, and 20 - §103(a) Rejection

Claims 1-2, 12-14, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Juniper ("Juniper Networks M40 Internet Backbone Router Inter-Operating With the CIENA MultiWave Sentry DWDM System") in view of the admitted prior art, Waschka, Jr. (U.S. Patent No. 4,449,247), Bach *et al.* (U.S. Patent No. 6,606,354), Bergano *et al.* ("Margin measurements in optical amplifier systems") and Hoogerbrugge ("Optimizing test strategies for SONET/SDH/ATM network element manufacturing").

First, Applicants respectfully submit that the Juniper reference is disqualified prior art pursuant to 35 U.S.C. §103(c). Specifically, this reference is a publication of Ciena Corporation, the assignee of the present application. Further, Applicant respectfully notes that the Juniper reference does not include a publication date. The Juniper reference does include dates of January 1999 on page 3 which are the dates the testing was performed at Ciena's validation labs. However, there is not a corresponding publication date listed on the reference

In Examiner's list of references (mail date 12/13/2005), Examiner states that the Juniper reference was accessed on 12/10/2005 at the following location on the Internet:

http://www.juniper.net/solutions/literature/interoperabiilty/ciena-mar99/interop.pdf

However, Applicants are unable to find the Juniper reference at this location. Accordingly, Applicants respectfully submit that the Juniper reference cannot be used as §102(a) or (b) prior art under MPEP §2128 (listed below).

> MPEP §2128 - Date of Availability
>
> Prior art disclosures on the Internet or on an on-line database are considered to be publicly available as of the date the item was publicly posted. *>Absent evidence of the date that the disclosure was publicly posted, if< the publication >itself< does not include a publication date (or retrieval date), it cannot be relied upon as prior art under 35 U.S.C. 102(a) or (b)*>. However<, it may be relied upon to provide evidence regarding the state of the art. Examiners may ask the Scientific and Technical Information Center to find the earliest date of publication >or posting<. See MPEP § 901.06(a), paragraph IV. G.

Applicants have a filing date on the present application of 04/17/2000. Examiner listed the publication date as 03/1999. However, this date is not included anywhere in the Juniper reference. Accordingly, the Juniper reference is disqualified under §103(c).

With regards to independent Claims 1 and 5, Applicants have amended the detecting step to recite (from Claims 1 and 5 respectively):

> detecting errors in the bit error rate test signal received by the bit error rate tester and calculating therefrom a measured system bit error rate **to simultaneously test the N optical communication channels for a time period, wherein the time period is a shorter time period relative to a time required to determine an actual bit error rate for the N optical communication channels**;

> detecting **one or more bit errors** and Q **to simultaneously test the said plurality of optical communication channels for a time period, wherein the time period is a shorter time period relative to a time required to determine an actual bit error rate for said plurality of optical communication channels,**

wherein the detecting is performed by a performance monitor in each of the optical transmitters and each of the optical receivers in the continuous cascade of a co-located plurality of optical transmitter/receiver pairs, wherein each performance monitor comprises an optical-to-electrical converter, a signal conditioning unit, an analog-to-digital converter, a microprocessor, a clock and data recovery unit, a decision circuit, and an error monitoring unit, and wherein each performance monitor actively monitors bit errors **by calculating Bit Interleave Parity for each frame and comparing it to a calculated Bit Interleave Parity for a next frame to detect if there are one or more bits errors in a particular communication channel** and Q by adjusting a decision level threshold provided by the microprocessor; and

As described on page 9 of the specification, Applicants are reducing testing time through cascading channels and testing for a short time period. Applicants are looking for even one single bit error, and that one bit error would denote a faulty channel. Here, Applicants are just looking to find which particular channels have errors on them with the corresponding performance monitors and diagnostic signals.

Examiner is not persuaded by Applicants previous amendments and arguments with respect to simultaneously testing and isolating errors. Examiner cites Waschka Jr. at col. 19, lines 30-59 for teaching the diagnostic signal functionality. However, Waschka Jr. teaches isolating the fault location through "sequential testing of the stations along the channel" (see Waschka Jr. at col, 19, lines 40-41). Applicants are unclear as how Waschka Jr. can be modified with Hoogerbrugge to provide fault isolation while simultaneously testing the communication channel in a cascaded fashion. Applicants respectfully agree that simultaneous testing is a suitable alternative to sequential testing; however, Applicants do not agree that the combination of references teach simultaneous testing cascaded channels while isolating faults to a specific channel at the same time.

Applicants respectfully submit that the performance monitor and diagnostic signals are not taught by Waschka Jr. Waschka Jr. only teaches sequential testing. The purpose of the performance monitor and the diagnostic signals is to enable the isolation of as few as one bit error in order to significantly reduce testing time and equipment. Waschka Jr. specifically teaches sequential testing. Accordingly, Waschka Jr. cannot teach the

performance monitor and diagnostic signals since these specifically function to enable simultaneous testing and isolation which Waschka Jr. specifically teaches against.

Additionally, Applicants have amended Claims 1 and 5 to include

> wherein each performance monitor actively monitors bit errors **by calculating Bit Interleave Parity for each frame and comparing it to calculated Bit Interleave Parity for a next frame**

With regard to independent Claim 9, Applicants have amended this Claim to recite the structural limitation associated with the present invention as discussed with the Examiner. Specifically, Claim 9 has been amended to recite:

> 9. A system for testing optical communication channels for wavelength division multiplexed optical communication, comprising:
>
> **a first set of optical transmitters and optical receivers at a first site;**
>
> **a second set of optical transmitters and optical receivers at a second site;**
>
> **optical fibers between the first site and the second site, wherein the first set of optical transmitters are connected to the second set of optical receivers over the optical fibers, and wherein the second set of optical transmitters are connected to the first set of optical receivers over the optical fibers;**
>
> **wherein each of the first set and the second set is configured in a cascaded configuration to define a single continuous communication path from an input of a first optical transmitter to an output of a last optical receiver through all the optical transmitters and all the optical receivers in the first set at the first site and in the second set at the second site and through the optical fibers;**
>
> a bit error rate tester to generate a bit error rate test signal, wherein the bit error rate–test signal is transmitted over **the single continuous communication path**;
>
> a performance monitor in each of the optical transmitters and each of the optical receivers, wherein each performance monitor comprises an optical-to-electrical converter **converting an input optical signal into an electrical signal**, a signal conditioning unit **conditioning the electrical signal**, an analog-to-digital converter, a microprocessor **calculating and saving Bit Interleave Parity for each frame**, a clock and data recovery unit **performing clock and data recovery**, a decision circuit **receiving Bit Interleave Parity for each frame from the clock and data recovery unit and a saved Bit Interleave Parity for each previous frame from the microprocessor**, and an error monitoring unit **incrementing a counter responsive to a difference from the decision circuit**

between the saved Bit Interleave Parity and the received Bit Interleave Parity, and wherein each performance monitor actively monitors bit errors **by calculating Bit Interleave Parity for each frame and comparing it to a calculated Bit Interleave Parity for a next frame to detect if there are one or more bits errors in a particular communication channel** and Q by adjusting a decision level threshold provided by the microprocessor; and

a diagnostic analyzer to analyze diagnostic output signals from **the decision circuit of each performance monitor** to identify at least one faulty communication channel **in the single continuous communication path**, and

wherein each of the diagnostic **output** signals from **the decision circuit** indicates a number of bit errors which were produced from a first optical transmitter up to and including a corresponding optical transmitter**/receiver associated with the decision circuit**; and

wherein the diagnostic output signals enable the **diagnostics analyzer** to isolate bit errors in **a particular communication channel of the single continuous communication path** while simultaneously testing the **single continuous communication path for a time period, wherein the time period is a shorter time period relative to a time required to determine an actual bit error rate for the single continuous communication path**.

Accordingly, Applicants respectfully submit the rejection has been traversed, and respectfully request withdrawal of this rejection.

Claims 3-11, 15-19, and 21-22 - §103(a) Rejection

Claims 3-11, 15-19, and 21-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Juniper in view of the admitted prior art, Waschka, Jr., Bach, Bergano *et al.*, and Hoogerbrugge as applied to Claim 1, and in further view of Bullock *et al.* (U.S. Patent No. 5,764,651). The amendments and remarks with regard to Claims 1, 5, and 9 apply with equal force here. Therefore, Applicants respectfully submit the rejection has been traversed, and respectfully request withdrawal of this rejection.

CONCLUSION

Applicants would like to thank Examiner for the attention and consideration accorded the present Application. Should Examiner determine that any further action is necessary to place the Application in condition for allowance, Examiner is encouraged to contact undersigned Counsel at the telephone number, facsimile number, address, or email address provided below. It is not believed that any fees for additional claims, extensions of time, or the like are required beyond those that may otherwise be indicated in the documents accompanying this paper. However, if such additional fees are required, Examiner is encouraged to notify undersigned Counsel at Examiner's earliest convenience.

Respectfully submitted,

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